

UTILITY PATENT APPLICATION TRANSMITTAL

Attorney Docket No.

851063.438

First Inventor or Application Identifier

Leonardo Fragapane

Title

ELECTRONIC SEMICONDUCTOR POWER DEVICE
WITH INTEGRATED DIODE

Express Mail Label No.

EL251278139US

Only for nonprovisional applications under 37 CFR § 1.53(b))

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 202311. ☐ General Authorization Form & Fee Transmittal
(Submit an original and a duplicate for fee processing)2. ☒ Specification [Total Pages] **10**
(preferred arrangement set forth below)

- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

☒ Drawing(s) (35 USC 113) [Total Sheets] **4**Oath or Declaration [Total Pages] **1**a. ☐ Newly executed (original or copy)b. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting
inventor(s) named in the prior application,
see 37 CFR 1.63(d)(2) and 1.33(b)

☐ Incorporation By Reference (useable if box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)7. Nucleotide and Amino Acid Sequence Submission
(if applicable, all necessary)a. ☐ Computer-Readable Copyb. ☐ Paper Copy (identical to computer copy)c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))9. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney10. ☐ English Translation Document (if applicable)11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations12. ☐ Preliminary Amendment13. ☒ Return Receipt Postcard14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)16. ☒ Other: Certificate of Express Mail

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information below and in a preliminary amendment

☐ Continuation ☐ Divisional ☐ Continuation-In-Part (CIP) of prior Application No.: _____

Prior application information: Examiner _____ Group / Art Unit _____

☒ Claims the benefit of European Patent Application No. EP99830023.0, filed January 25, 1999

CORRESPONDENCE ADDRESS

E. Russell Tarleton
Seed Intellectual Property Law Group PLLC
701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900 / Fax: (206) 682-6031

Respectfully submitted,

TYPED or PRINTED NAME E. Russell TarletonSIGNATURE E. Russell Tarleton

U:\KristineO\ERT\40-cover.doc

REGISTRATION NO. 31,800Date January 25, 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Leonardo FRAGAPANE
Filed : January 25, 2000
For : ELECTRONIC SEMICONDCUTOR POWER DEVICE WITH
INTEGRATED DIODE

Docket No. : 851063.438

Date : January 25, 2000

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Assistant Commissioner for Patents:

I hereby certify that the enclosures listed below are being deposited with the United States Postal Service "EXPRESS MAIL Post Office to Addressee" service under 37 C.F.R. § 1.10, Mailing Label Certificate No. EL251278139US, on January 25, 2000, addressed to Box Patent Application, Assistant Commissioner for Patents, Washington, DC 20231.

Respectfully submitted,

Seed Intellectual Property Law Group PLLC



Kristine K. Houston

Enclosures:

Postcard
Form PTO/SB/05
Specification, Claims, Abstract (10 pages)
4 Sheets of Drawings (Figures 1-9)

U:\KristineO\ERT\41-expressmail.doc

005270 63506100

ELECTRONIC SEMICONDUCTOR POWER DEVICE WITH INTEGRATED DIODE

TECHNICAL FIELD

The present invention relates to an electronic semiconductor device having a modified insulated gate bipolar transistor with integrated diode.

5 BACKGROUND OF THE INVENTION

A known electronic device is a transistor of the type called IGBT (Insulated Gate Bipolar Transistor). IGBT devices are components used in power applications as an alternative to bipolar junction transistors (BJT) or field-effect power transistors, such as vertical conduction transistors, known as VDMOS (Vertical Double diffused Metal Oxide Semiconductor) transistors. They are sometimes preferred to BJT and VDMOS transistors because they have a smaller size with the same electrical performance. In some applications, however, VDMOS transistors are more advantageous than IGBT devices because they contain, as a component intrinsic to their structure, a reverse diode between the drain and source. A typical application in which this characteristic of the VDMOS is exploited is that in which the power device is used as an electronic switch in a bridge or half-bridge circuit configuration. In this configuration, the diode allows current to flow when the power device is biased in the reverse conduction direction. If an IGBT is to be used as an electronic switch in this circuit configuration, it is necessary to connect a separate diode between its emitter and collector terminals. This results in a greater complexity of construction and a larger size of the whole device.

It has been proposed that an IGBT be modified in such a way that a structure normally present in this device is used as a reverse diode. An IGBT modified in this way is described below in relation to Figure 1.

Figure 1 shows in section an edge portion of a chip 9 of semiconductor material, for example monocrystalline silicon. The chip 9 comprises a substrate 10 doped with P type impurities in a relatively high concentration, and consequently denoted by P+, an epitaxial layer 11 doped with N type impurities in a relatively low concentration, and

consequently denoted by N-, and an N+ "buffer" layer 12 between the substrate 10 and the epitaxial layer 11. (The buffer layer may also be absent in certain types of IGBT). A diffused P type region 13 extends from the front surface of the chip 9 into the epitaxial layer 11 and is formed by a low-concentration (P-) surface part 13' and a high-
5 concentration (P+) deep part 13". Another P type region, indicated by 14, also formed by a low-concentration part 14' and a high-concentration part 14", is shaped in such a way that it surrounds the region 13.

High-concentration N type regions 15 are formed in the regions 13 and 14. Strips of electrically conducting material, for example doped polycrystalline silicon,
10 indicated by 16, separated from the front surface of the chip by a thin layer of dielectric material, for example silicon dioxide, are located above the surface areas of the regions 13' and 14' lying between the regions 15 and the epitaxial layer 11. The strips 16 are joined together (in a way not shown in the drawing) in a structure which also comprises a contact portion 16'. A metallic electrode 17 in contact with the bottom surface of the chip, in other
15 words with the free surface of the substrate 10, forms the collector electrode C of the transistor. A metallic electrode 18 in contact, on the front surface, with the P+ regions 13 and 14 and with the N+ regions 15, but insulated from the strips 16 by layers of dielectric material 19, for example silicon dioxide, forms the emitter electrode E of the IGBT. A metallic electrode 20 in contact with the contact portion 16' forms the gate electrode of the
20 IGBT.

It should be noted that two separate electrodes, one in contact with the region 13 and one in contact with the region 14, but connected electrically to each other by a suitable connecting element, could be provided instead of a single electrode 18 in contact with the regions 13 and 14. A further metallic electrode 21 forms an ohmic contact with
25 the epitaxial layer 11 through a diffused high-concentration N type surface region, indicated by 22, and is shaped in the form of a frame extending close to the edge of the chip. This electrode is also connected, by a conductor external to the chip 9, to the collector electrode 17 of the IGBT.

Figure 2 shows in a plan view, and not to scale, the chip 9 fixed to a metallic support 23 and connected electrically to three terminals of the device. More in particular, one of the three terminals, indicated by 24, is soldered to the metallic support 23, the collector electrode 17 is soldered to the metallic support 23 and is therefore connected
5 electrically to the terminal 24, the emitter electrode 18 and the gate electrode 20 are connected by corresponding metal wires to the other two terminals 25 and 26, and the electrode 21 is connected by a wire to the terminal 24.

In operation, when a potential which is positive with respect to that of the emitter is applied to the collector, and the gate electrode is biased, with respect to the
10 emitter electrode, at a potential greater than the conduction threshold level, a current flows from the emitter to the collector, as indicated by arrows in the Figure. Conversely, when the gate electrode is biased at a potential lower than the conduction threshold level, no current passes between the emitter and the collector and the device therefore acts as an open switch. The maximum voltage that can be applied between the collector and the
15 emitter is determined by the breakdown voltage of the junctions which the regions 13 and 14 form with the epitaxial layer 11. The region 14 surrounds the whole active region of the device in the same way as a frame, and its low-concentration surface part 14' which extends laterally towards the edge of the chip makes it possible to obtain a breakdown voltage close to the theoretical level, owing to the known effect of reduction of the density
20 of the field lines at the surface. The electrode 21, which is not normally connected to the collector electrode, is used to keep the whole edge area of the chip at the same potential, and is therefore usually called an equipotential ring or EQR. This has the effect of maintaining a uniform breakdown voltage over the whole chip. The combination of the region 14 and the electrode 21 is normally called an edge structure or a termination
25 structure.

Since the electrode 21 is connected to the collector C, when the IGBT is reverse-biased, in other words when the collector has a negative potential with respect to the emitter, the diode formed by the p-n junction between the region 14 and the epitaxial layer 11, in other words between the emitter electrode and the electrode 21, indicated by D

in Figure 1, is conducting. The IGBT can therefore be used in a bridge or in a half-bridge in the applications described above.

However, it has been found that the diode thus formed has a high resistance in forward conduction, and therefore the voltage drop across its terminals is high even with
5 relatively low currents, for example more than 5 V for a current of 0.4 A, whereas a drop of approximately 2 V, like that of the IGBT in forward conduction, would be desirable. Moreover, the characteristics of the diode cannot be improved beyond a certain limit because they depend on parameters which cannot be modified without altering the characteristics of the IGBT, such as the perimeter of the termination region 14, the distance
10 between the EQR electrode 21 and the P+ part 14" of the region 14, and the width of the P-region 14'.

SUMMARY OF THE INVENTION

The present invention provides an electronic device of the type described above having an integrated diode with operating characteristics.

15 BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more clearly understood from the following detailed description of some embodiments of the invention, provided with reference to the attached drawings, in which:

Figure 1 is a section through a portion of a chip of semiconductor material
20 containing a known device,

Figure 2 shows in plan view, and not to scale, the chip in Figure 1 mounted on a supporting structure,

Figure 3 is a section through a portion of a chip of semiconductor material containing a device according to the invention,

25 Figure 4 shows in plan view, and not to scale, of the chip in Figure 3 mounted on a supporting structure,

Figure 5 shows an equivalent circuit diagram of the device according to the embodiments shown in Figures 3 and 4,

Figure 6 is a section through a portion of a chip of semiconductor material, which shows a variant of the device according to the invention,

5 Figures 7 and 8 show, in section and in plan view respectively, a device according to another embodiment of the invention, and

Figure 9 is a section through a portion of a chip of semiconductor material containing a device according to a further embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

10 The device shown in Figures 3 and 4, in which elements identical to those of the structure in Figures 1 and 2 are denoted by the same reference numbers, differs in one respect from the known device in that the termination structure comprises, between the termination region 14 and the EQR electrode 21, a further electrode 30 in ohmic contact with the epitaxial layer 11 through a diffused high-concentration N type region 31, and a
15 further P type termination region 32, formed by a low-concentration surface part 32' and a high-concentration deep part 32" and having a surface contact electrode 33.

As shown in plan view in Figure 4, the electrode 30 surrounds, in the form of a frame, the active part of the device comprising the region 13 and any other P type regions identical to the region 13. The second termination region 32 is also shaped in the
20 form of a frame which surrounds the electrode 30. The electrodes 18 and 33 are connected, by a metal wire in each case, to the emitter terminal 25 of the device, and the electrodes 21 and 30 are connected, by a metal wire in each case, to the collector terminal 24 of the device.

Preferably, the regions 13, 14 and 32 are formed simultaneously by the same
25 operations of photographic processes, implantation and diffusion. The same is true of the N+ regions 22 and 31. The improved structure according to Figures 3 and 4 is therefore obtained without any supplementary operation.

As shown in Figure 3 and in Figure 5, the new termination structure comprises three diodes D1, D2, D3 connected electrically between the emitter and collector terminals of the IGBT in parallel with each other and in the direction of conduction opposite that of the IGBT. Each of the three diodes has electrical characteristics substantially equivalent to those of the diode D according to the known art, since, for an equal distance between the N+ cathode contacts and the P+ anode region, the forward diode current depends on the perimeter of the regions which form its junction. The total forward current of the three diodes is therefore three times greater than that of the diode according to the known structure.

According to a variant of the invention shown in Figure 6, in which elements identical or equivalent to those of Figure 3 are denoted by the same reference numbers, the low-concentration surface parts 14' and 32' of the two termination regions 14 and 32 are combined in a single region and the diffused high-concentration N type region extends in this single region. This variant is particularly advantageous in the case in which the metallic element 18 which is in surface contact with the regions 13 and 14 is interdigitated with the electrode 30. In this way, the perimeter of the regions which form the reverse diode can be made as large as necessary by appropriate selection of the number of projections of the interdigitated structure, without adversely affecting the performance of the IGBT in terms of the breakdown voltage. A structure of this type is shown in section and in plan view in Figures 7 and 8 respectively, in which elements identical or equivalent to those of Figures 3, 4 and 6 are denoted by the same reference numbers.

The invention can be applied advantageously in all types of IGBT to be used in circuit configurations in which a reverse diode is necessary. When the IGBT has to be used as a high-frequency switch, there is a known arrangement of uniformly implanting and diffusing doping species, such as platinum or protons, capable of reducing the lifetime of the charge carriers, into the chip. This arrangement, however, has a negative effect on the diode, since it reduces the charge injection efficiency. To avoid this negative effect, according to an embodiment of the invention shown in Figure 9, a buried layer 38 is formed, and the doping species capable of reducing the lifetime of the carriers are placed in

it. In the structure shown, identical to that of Figure 3 except for the presence of the buried layer, atoms, of helium for example, are implanted before or after the phase of epitaxial growth of the layer 11. The buried layer 38 is formed above the N+ "buffer" layer 12. In cases in which the buffer layer is not provided, the implantation takes place on the surface
5 of the substrate 10 before the phase of epitaxial growth.

In operation, the buried layer 38 performs its function of improving the high-frequency performance of the IGBT by reducing its decay time, but has no effect on the performance of the diode in forward conduction, since the forward current of the diode is virtually exclusively of the lateral type; in other words, it flows parallel to the surface of
10 the chip and close to the surface.

It is clear from the above description that the electronic device contains an integrated diode having electrical characteristics that are markedly better than those of the known integrated diode. In particular, the voltage drop obtained across the diode in forward conduction is very close to that of the IGBT in conduction, for virtually any
15 operating current of the device.

Although the invention has been illustrated and described with reference to an IGBT formed on a P+ substrate, it should be understood that it can also be applied on an N+ substrate; clearly, in this case, the type of conductivity of all the layers and all the regions would be complementary. It should also be understood that the invention can
20 additionally be applied advantageously in devices of types other than the IGBT, for example in bipolar junction power transistors to be used as electronic switches in bridge or half-bridge configurations.

CLAIMS

1. An electronic device formed on a chip of semiconductor material (9) comprising:

a substrate having a first type of conductivity and a plurality of surfaces, one of whose surfaces is a bottom surface of the chip,

a layer having a second type of conductivity formed on the substrate and having a surface which is a top surface of the chip,

at least one first region having the first type of conductivity, that extends into the layer from the top surface,

a termination structure comprising:

a first termination region having the first type of conductivity, that extends into the layer from the top surface and is shaped in such a way that it surrounds the at least one first region,

a first electrode in contact with the first termination region,

a second electrode in contact with the layer on the top surface, shaped in the form of a frame close to the edge of the chip,

a third electrode in contact with the bottom surface of the chip and connected electrically to the second electrode,

a fourth electrode in contact with the at least one first region and connected electrically to the first electrode,

a fifth electrode in contact with the layer on the top surface along a path that extends substantially parallel to at least part of an edge of the first termination region and connected electrically to the second electrode,

a second termination region having the first type of conductivity, which extends into the layer from the front surface, and shaped in the form of a frame surrounding the fifth electrode, and

a sixth electrode in contact with the second termination region and connected electrically to the first electrode.

2. The device of claim 1 wherein the each of the first and the second termination regions comprises a low-concentration surface part and a high-concentration deep part.

3. The device of claim 2 wherein the low-concentration surface parts of the first and the second termination regions are combined in a single region and wherein the termination structure comprises a region having the second type of conductivity at high concentration that extends into the surface parts common to the first and the second termination regions from the portion of the front surface of the chip with which the fifth electrode is in contact.

4. The device of claim 1 wherein the first and the fourth electrodes comprise a single metallic element.

5. The device of claim 1 in which the path along which the fifth electrode extends is shaped in the form of a frame that encloses the at least one first region.

6. The device of claim 4 wherein the metallic element and the fifth electrode are interdigitated.

7. The device of the claim 1 wherein the chip of semiconductor material comprises a buried layer containing doping species that reduce the lifetime of the charge carriers.

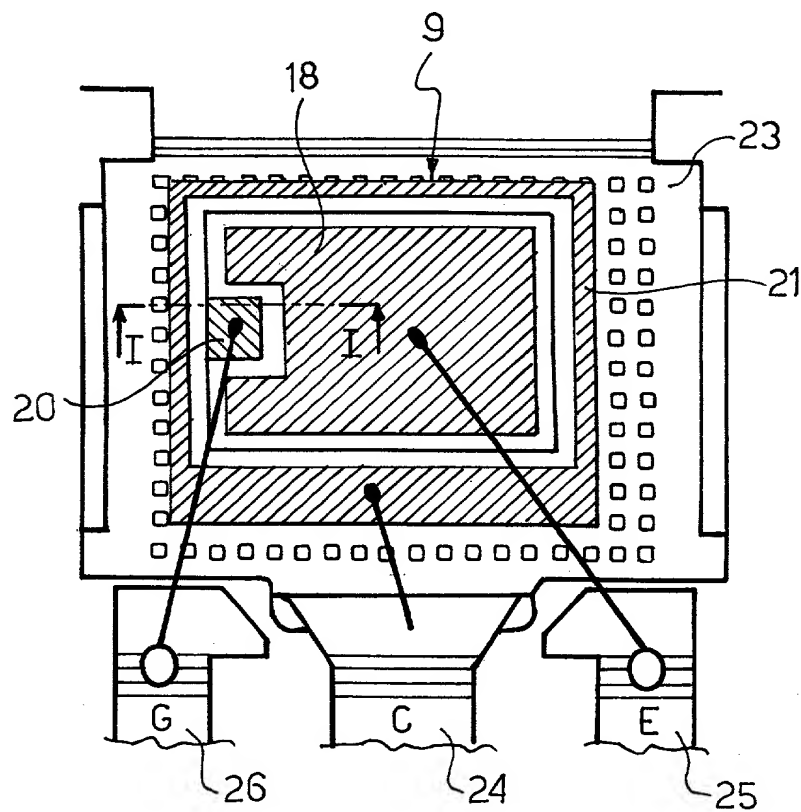
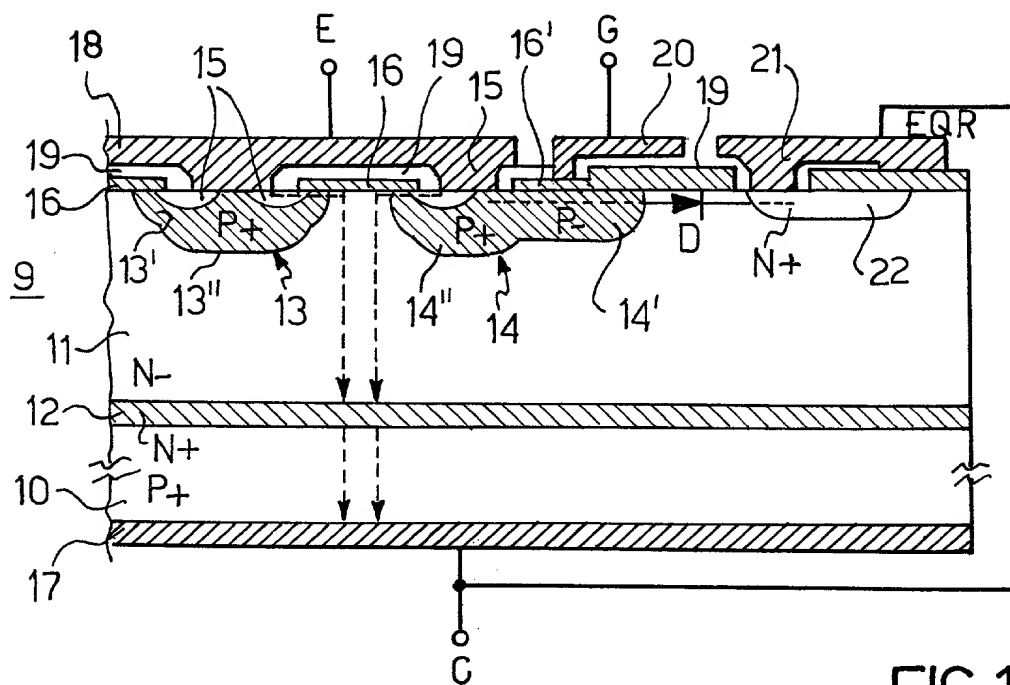
8. The device of claim 7 wherein the doping species comprise helium atoms.

ELECTRONIC SEMICONDUCTOR POWER DEVICE WITH INTEGRATED DIODE

ABSTRACT OF THE DISCLOSURE

A device including an IGBT a formed on a chip of silicon consisting of a P type substrate with an N type epitaxial layer that contains a first P type region and a termination structure, and having a first P type termination region that surrounds the first region, a first electrode in contact with the first termination region, and a second electrode shaped in the form of a frame close to the edge of the chip and connected to a third electrode in contact with the bottom of the chip. A fourth electrode made in one piece with the first electrode is in contact with the first region. The termination structure also comprises a fifth electrode in contact with the epitaxial layer along a path parallel to the edge of the first termination region and connected to the second electrode and a second P type termination region that surrounds the fifth electrode and a sixth electrode, and which is in contact with the second termination region, connected to the first electrode.

WPN/851063/438-AP



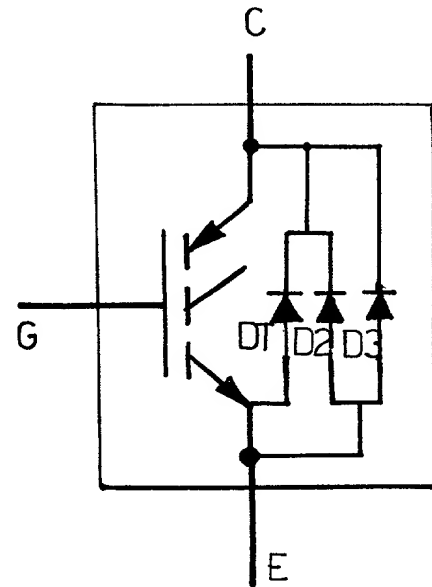
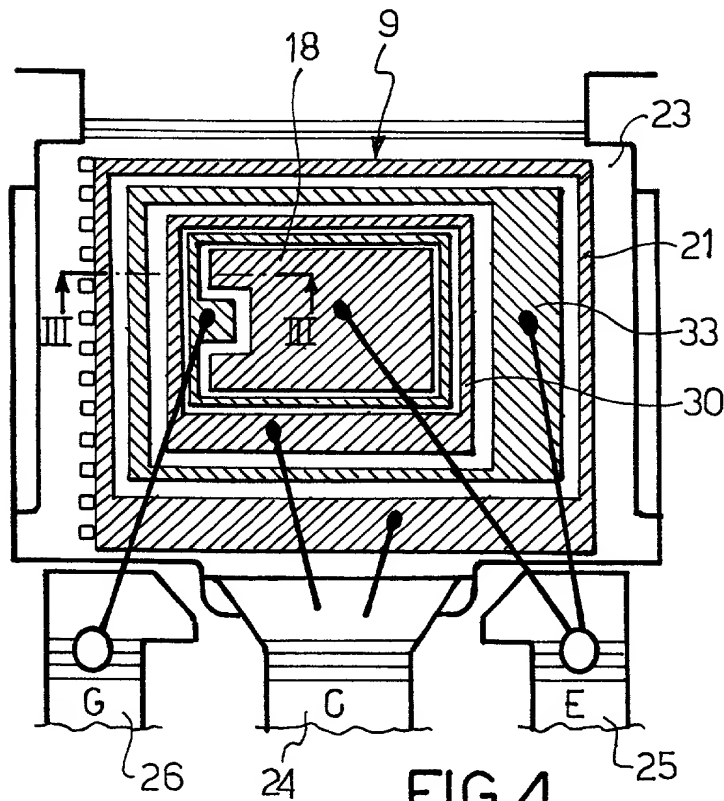


FIG.5

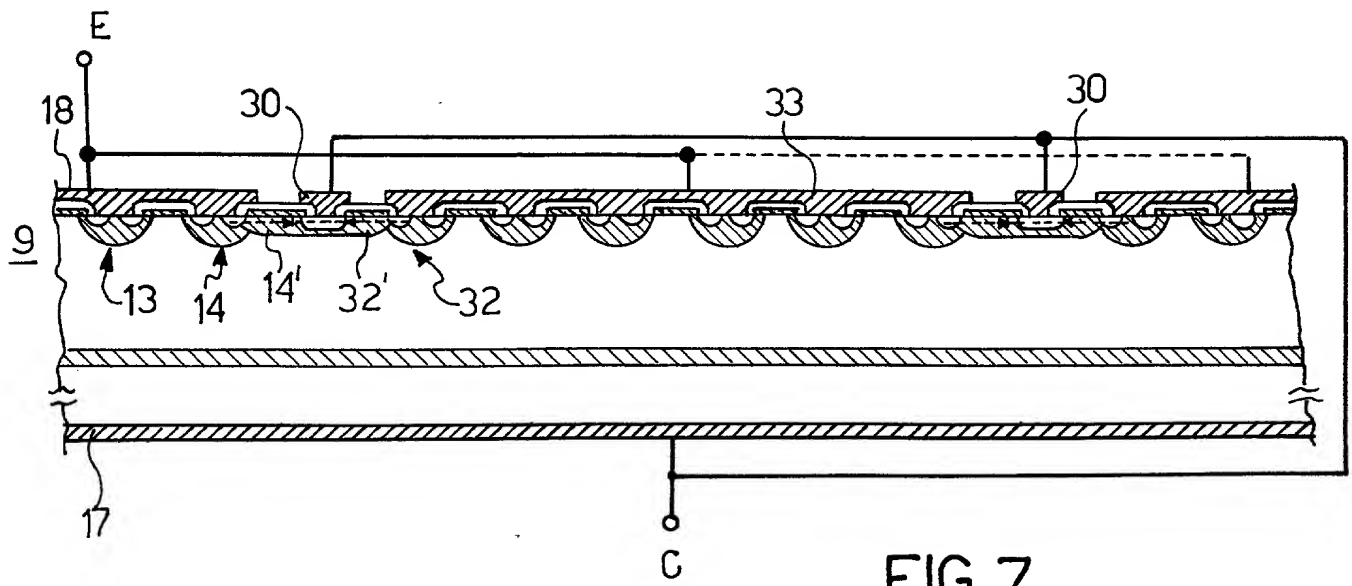


FIG. 7

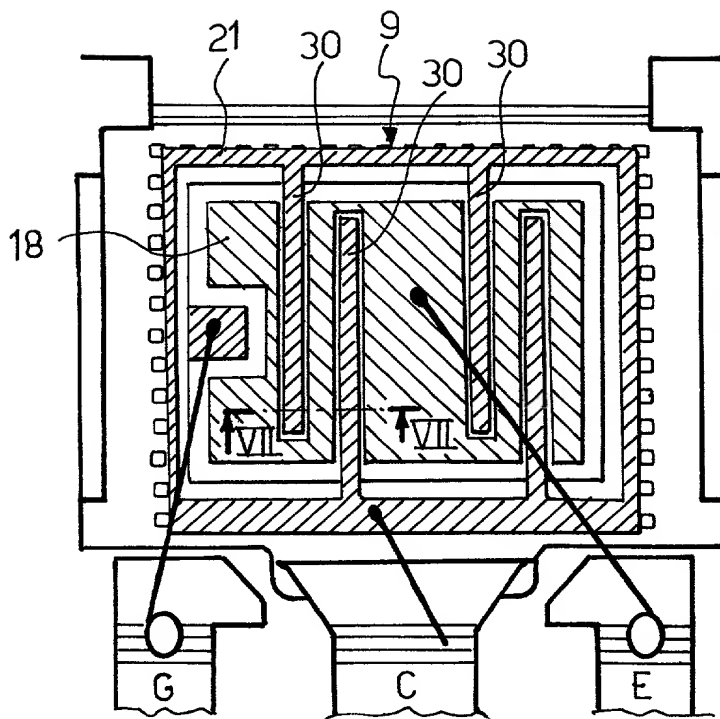


FIG. 8

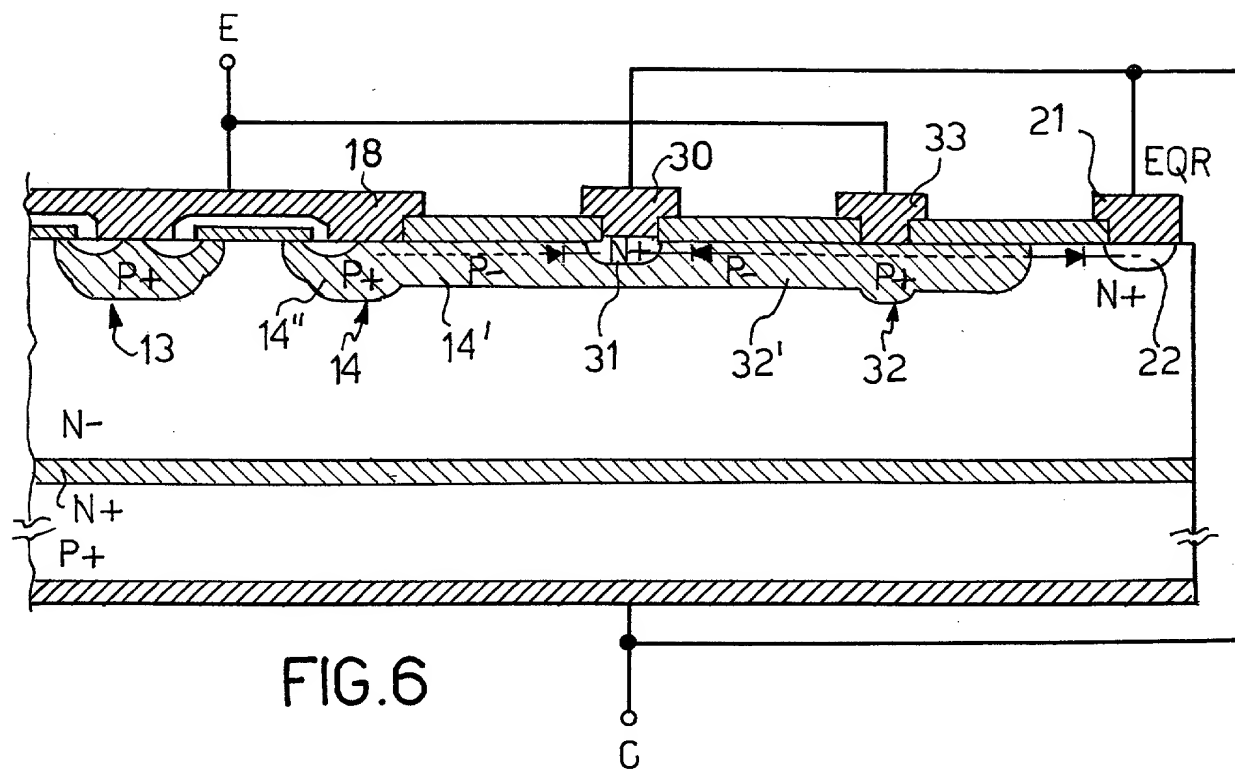


FIG. 6

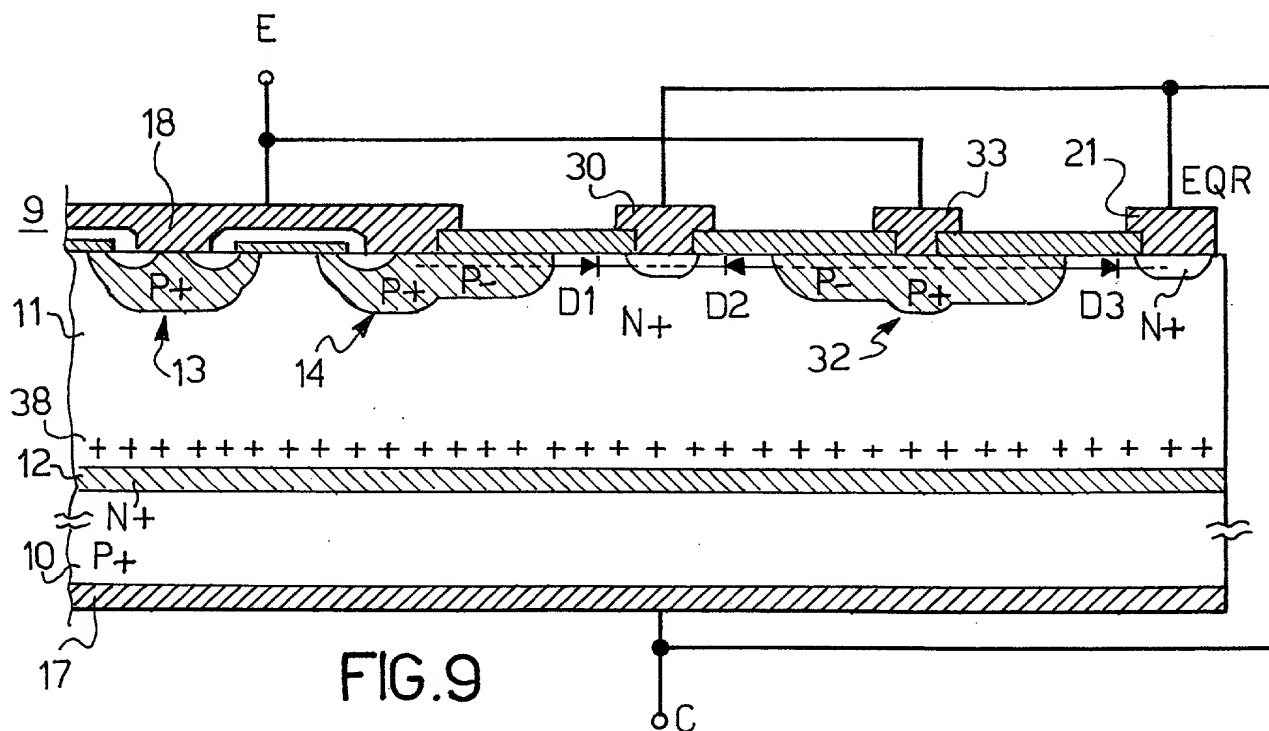


FIG. 9